

1154.41135X00  
15524S

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Marko KARPPANEN  
Filed: February 13, 2002  
For: METHOD AND DEVICE FOR IMPROVING THE  
RELIABILITY OF A COMPUTER SYSTEM

**PRELIMINARY AMENDMENT**

Assistant Commissioner of Patents  
Washington, D.C. 20231

February 13, 2002

Sir:

Please enter the following preliminary amendments and remarks as follows:

**IN THE SPECIFICATION:**

**After the title of the invention insert:**

**CROSS REFERENCE TO RELATED APPLICATION:**

This application is a continuation of PCT Application FI00/00689.

**Please replace the paragraph beginning at page 1, line 3, with the following rewritten paragraph:**

**BACKGROUND OF THE INVENTION**

Field of the Invention

The present invention relates to computer systems. In particular, the invention concerns a method and device for improving the reliability of a computer system.

**Please replace the paragraph beginning at page 1, line 7, with the following rewritten paragraph:**

### Description of the Prior Art

In computer systems, standardized bus solutions are used to interconnect different peripherals or processor systems. CompactPCI (PCI, Peripheral Component Interconnect) is a bus solution based on the PCI bus, used especially in computer systems intended for industrial and/or embedded applications in mechanically demanding environments. A more extensive description of the properties of the PCI bus is to be found in the publication "PCI Local Bus Specification", PCI Special Interest Group, June 1, 1995. We incorporate the publication into the present application by reference in its entirety.

**Please replace the paragraph beginning at page 2, line 16, with the following rewritten paragraph:**

### SUMMARY OF THE INVENTION

The present invention eliminates the problems described above or at least significantly alleviates them. The invention is also a new type of method and device for disconnecting a defective unit from a computer system in the event of a fault. The invention also improves the reliability of the PCI bus system by using a simple monitoring mechanism working internally in the device connected to the bus.

**Please replace the paragraph beginning at page 5, line 6, with the following rewritten paragraph:**

### BRIEF DESCRIPTION OF THE DRAWINGS

**Please replace the paragraph beginning at page 5, line 11, with the following rewritten paragraph:**

Figs. 1a and 1b present diagrams representing an embodiment of the system of the invention;

Please replace the paragraph beginning at page 8, line 8, with the following rewritten paragraph:

Fig. 2 presents an example giving a more detailed representation of the components shown in Figs. 1a and 1b. Fig. 2 illustrates the components and signaling in the interface circuit of a plug-in unit or interface unit at block diagram level. The interface circuit is connected to a CompactPCI bus (CompactPCI BUS). The operation and function of these components are obvious to the skilled person and therefore are not described in detail except for parts that are significant in respect of the invention. The watchdog timer (Fig. 2) is started when an addressing sequence in the PCI bus begins, i.e. when a plug-in unit behind an interface circuit is addressed via the bus. The interface circuit detects the addressing e.g. by an active IDSEL signal indicating the selection of a plug-in unit.

#### **IN THE CLAIMS:**

Please cancel claims 1-8 and substitute therefore the following new claims 9-17.

9. A method for improving the reliability of a computer system including a bus, an interface circuit, and a plug-in unit which is connected to the bus via the interface circuit comprising:

addressing the plug-in unit via the bus by addressing operations directed at the plug-in unit which are monitored by the interface circuit;

measuring a duration of addressing of the plug-in unit; and when

the duration exceeds a predetermined period of time, then the addressing is terminated by sending into the bus a signal indicating termination of addressing.

10. A method as defined in claim 9, wherein:

the duration of addressing is monitored using a watchdog timer with a predetermined timing set therein.

11. A method as defined in claim 9, wherein:

when addressing is terminated an error signal is set by the interface circuit into an active state in the bus.

12. A method as defined in claim 9, wherein:

when addressing is terminated an error signal indicating an error condition in the plug-in unit is set by the interface circuit into an active state in the status register of the plug-in unit.

13. An interface circuit for improving the reliability of a computer system including a bus, and a plug-in unit which is connected to the bus via the interface circuit, the interface circuit comprising:

a watchdog timer;

means for starting the watchdog timer upon the start of addressing; and

means for sending into the bus a signal indicating termination of addressing.

14. An interface circuit as defined in claim 13, comprising:

means for setting an error signal into an active state in the bus.

15. An interface circuit as defined in claim 13, comprising:

means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit.

16. An interface circuit as defined in claim 14 comprising:

means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit.

17. An interface circuit as defined in claim 13, where:

the bus is a CompactPCI bus.

1154.41135X00  
15524S


**REMARKS**

The specification and claims have been amended to improve their form for examination and to eliminate multiple dependent claims for fee calculation purposes.

To the extent necessary, please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (1154.41135X00)

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

  
\_\_\_\_\_  
Donald E. Stout, Registration No.26,422

DES:dmw  
(703) 312-6600 – phone  
(703) 312-6666 – fax  
dstout@antonelli.com - e-mail

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE SPECIFICATION:**

Please replace the paragraph beginning at page 1, line 3, with the following rewritten paragraph:

**BACKGROUND OF THE INVENTION**

**Field of the Invention**

The present invention relates to computer systems. In particular, the invention concerns a method and device for improving the reliability of a computer system.

Please replace the paragraph beginning at page 1, line 7, with the following rewritten paragraph:

**[BACKGROUND OF THE INVENTION]**

**Description of the Prior Art**

In computer systems, standardized bus solutions are used to interconnect different peripherals or processor systems. CompactPCI (PCI, Peripheral Component Interconnect) is a bus solution based on the PCI bus, used especially in computer systems intended for industrial and/or embedded applications in mechanically demanding environments. A more extensive description of the properties of the PCI bus is to be found in the publication "PCI Local Bus Specification", PCI Special Interest Group, June 1, 1995. We [append] incorporate the publication into [to] the present application [via this] by reference in its entirety.

Please replace the paragraph beginning at page 2, line 16, with the following rewritten paragraph:

**SUMMARY OF THE INVENTION**

The [object of the] present invention [is to eliminate] eliminates the problems described above or at least [to] significantly [alleviate] alleviates them. [A further object of the] The invention is [to disclose] also a new type of method and device for disconnecting a defective unit from a computer system in the event of a fault. [Another object of the] The invention [is to improve] also improves the reliability of the PCI bus system by using a simple monitoring mechanism working internally in the device connected to the bus.

#### **[BRIEF DESCRIPTION OF THE INVENTION]**

**Please replace the paragraph beginning at page 5, line 6, with the following rewritten paragraph:**

#### **[LIST OF ILLUSTRATIONS] BRIEF DESCRIPTION OF THE DRAWINGS**

**Please replace the paragraph beginning at page 5, line 11, with the following rewritten paragraph:**

[Fig.]Figs. 1a and 1b present diagrams representing an embodiment of the system of the invention;

**Please replace the paragraph beginning at page 8, line 8, with the following rewritten paragraph:**

Fig. 2 presents an example giving a more detailed representation of the components shown in [Fig.] Figs. 1a and 1b. Fig. 2 illustrates the components and [signalling] signaling in the interface circuit of a plug-in unit or interface unit at block diagram level. The interface circuit is connected to a CompactPCI bus (CompactPCI BUS). The operation and function of these components are obvious to the skilled person and therefore [we shall] are not [describe them] described in detail except for parts that are significant in respect of the invention. The watchdog timer (Fig. 2) is



1154.41135X00  
15524S

started when an addressing sequence in the PCI bus begins, i.e. when a plug-in unit behind an interface circuit is addressed via the bus. The interface circuit detects the addressing e.g. by an active IDSEL signal indicating the selection of a plug-in unit.

1154.41135X00  
15524S